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PATENT
Attorney Docket No.: SAM-0474

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Kyoung-hwan Kwon, *et al.* Examiner: Wells, Kenneth B.
Serial Number: 10/671,105 Group Art Unit: 2816
Filing Date: September 25, 2003
Title: SEMICONDUCTOR DEVICE COMPRISING FREQUENCY MULTIPLIER OF EXTERNAL CLOCK AND OUTPUT BUFFER OF TEST DATA AND SEMICONDUCTOR TEST METHOD (as amended)

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited with the United States Post Office as First Class Mail in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

3-16-05
Date

Vanessa Marakas

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

RESPONSE TO RESTRICTION REQUIREMENT WITH PRELIMINARY AMENDMENT

Sir:

In response to the Restriction Requirement dated February 17, 2005 in the above-referenced patent application, the Applicants hereby elect Group III, including claims 16-21, without traverse.

Prior to prosecution on the merits, please amend the application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 10 of this paper.

Adjustment Date: 11/03/2005 SDIRETA1
04/07/2005 CPARIS 00000008 501798 10671105
01 FC:1251 120.00 CR

04/07/2005 CPARIS 00000008 501798 10671105
01 FC:1251 120.00 DA

MILLS & ONELLO LLP

ATTORNEYS AT LAW
INTELLECTUAL PROPERTY LAW

ELEVEN BEACON STREET, SUITE 605
BOSTON, MASSACHUSETTS 02108
E-MAIL: MAIL@MILLSONELLO.COM
WWW.MILLSONELLO.COM

TELEPHONE: (617) 994-4900

FACSIMILE: (617) 742-7774

August 22, 2005

Director of United States Patent and Trademark Office
Attention: Deposit Account
2051 Jamieson Avenue, Suite 300
Alexandria, Virginia 22314

Re: U.S. Patent Application No. 10/671,105
Our Reference: SAM-0474
Deposit Account No.: 501798

Dear Sirs:

After reviewing our April 2005 Monthly Statement of Deposit Account (copy attached), we noticed a charge in the amount of $120 in the referenced patent application. The fee code 1251 indicates that the charge was for an extension of time for response within the first month. We believe this charge is in error, and we request that the charge be reimbursed to us in the form of a credit to our deposit account.

On March 16, 2005, a Response to Restriction Requirement with a Preliminary Amendment was filed in the referenced application (copy attached), responding to an Election/Restriction mailed on February 17, 2005 (copy attached). The Response was filed within the designated one-month period for reply, as it was deposited in the U.S. Post Office in compliance with 37 C.F.R.§1.8 on March 16, 2005. No extensions of time were believed to be necessary at the time of filing the Response.

We ask that you review the enclosed and that our deposit account 501798 be credited in the amount of $120. Please feel free to contact us if we can answer any questions regarding this matter.

Very truly yours,

MILLS & ONELLO LLP

Anthony P. Onello, Jr.

APO/las
Enclosures
J:\SAM\0474\depaccountltr.wpd

United States Patent and Trademark Office

USPTO Home Page

Finance Online Shopping Page

Deposit Account Statement

Requested Statement Month:	April 2005
Deposit Account Number:	501798
Name:	MILLS & ONELLO LLP
Attention:	LISA A SANDERS
Address:	ELEVEN BEACON STREET
City:	BOSTON
State:	MA
Zip:	02108
Country:	UNITED STATES OF AMERICA

DATE	SEQ	POSTING REF TXT	ATTORNEY DOCKET NBR	FEE CODE	AMT	BAL
04/01	160	11040808	SAM-0623	8007	$100.00	$10,820.00
04/04	181	11095187		9204	-$1,200.00	$12,020.00
04/07	11	10671105	SAM-0474	1251	$120.00	$11,900.00
04/18	17	11044422	SAM-0616	8007	$20.00	$11,880.00
04/18	20	60643730	SAM-0701PR	8007	$20.00	$11,860.00
04/18	23	11044135	SAM-0617	8007	$40.00	$11,820.00
04/20	180	6328096	TMP-0016CIP	2551	$450.00	$11,370.00
04/22	444	11082497	SAM-0624	8007	$80.00	$11,290.00
04/26	26	11067836	SAM-0618	8007	$40.00	$11,250.00

START BALANCE	SUM OF CHARGES	SUM OF REPLENISH	END BALANCE
$10,920.00	$870.00	$1,200.00	$11,250.00

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,105	09/25/2003	Kyoung-Hwan Kwon	SAM-0474	7243

7590 02/17/2005

Anthony P. Onello, Jr.
MILLS & ONELLO LLP
Suite 605
Eleven Beacon Street
Boston, MA 02108

EXAMINER	
WELLS, KENNETH B	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 02/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,105	KWON ET AL.	
	Examiner	Art Unit	
	Kenneth B. Wells	2816	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2004*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-27* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Applicant's election of Group II in the 12/1/04 response is noted.

2. Upon further review, the examiner notes that previously identified Group II actually contains two patentably distinct inventions itself, i.e., claims 13-15 which are directed to a subcombination (data buffer), whereas claims 16-21 are directed to a combination (a data buffer together with a frequency multiplier). Note further evidence claim 16 (it is evidence that the combination claims 16-21 are separately patentable from the subcombination claims 13-15) and the fact that the subcombination data buffer of claims 13-15 has separate utility.

Thus, the three originally filed separately patentable groups are as follows:

Group I: claims 1-12 and 22-27 (subcombination frequency multiplier);

Group II: claims 13-15 (subcombination data buffer); and

Group III: claims 16-21 (combination of a data buffer together with a frequency multiplier).

3. Applicant's election of one of these three groups is required, since the first two are subcombinations usable

together and patentably distinct, and the second two are combination/subcombination and also patentably distinct.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (571)272-1757. The examiner can normally be reached on Monday through Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached at (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kenneth B. Wells
Primary Examiner
Art Unit 2816

February 17, 2005

Mailed on March 16, 2005 SAM-0474

Enclosed are the following in re:
Patent Appln of Kyoung-hwan Kwon, *et al.*
Serial No.: 10/671,105
Filed: September 25, 2003

SEMICONDUCTOR DEVICE COMPRISING FREQUENCY MULTIPLIER OF EXTERNAL CLOCK AND OUTPUT BUFFER OF TEST DATA AND SEMICONDUCTOR TEST METHOD (as amended)

1. Transmittal Letter
2. Amendment Transmittal
3. Response to Restriction Requirement with Preliminary Amendment

APO/vkm

This paper was received by the United States Patent and Trademark Office on:

Mailed on March 16, 2005 SAM-0474

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This paper was received by the United States Patent and Trademark Office on:

PATENT
Attorney Docket No.: SAM-0474
Customer No.: 29344

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Kyoung-hwan Kwon, *et al.*	Examiner: Wells, Kenneth B.
Serial Number:	10/671,105	Group Art Unit: 2816
Filing Date:	September 25, 2003	
Title:	SEMICONDUCTOR DEVICE COMPRISING FREQUENCY MULTIPLIER OF EXTERNAL CLOCK AND OUTPUT BUFFER OF TEST DATA AND SEMICONDUCTOR TEST METHOD (as amended)	

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3-16-05
Date

Vanessa Marakas

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

TRANSMITTAL LETTER

Sir:

Enclosed herewith for filing in the above-identified patent application please find the following:

1. Amendment Transmittal;
2. Response to Restriction Requirement mailed on February 17, 2005 with Preliminary Amendment; and
3. Return Postcard.

In connection with the foregoing matter, please charge any additional fees which may be due, or credit any overpayment, to Deposit Account Number 50-1798. A duplicate copy of this letter is provided for this purpose.

Respectfully submitted,

Date: March 16, 2005

MILLS & ONELLO LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900
Facsimile: (617) 742-7774

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Anthony P. Onello, Jr.
Registration Number 38,572
Attorney for Applicant

PATENT
Attorney Docket No.: SAM-0474
Customer No.: 29344

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Date: March 14, 2005

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Anthony P. Onello, Jr.
Registration Number 38,572
Attorney for Applicant

PATENT
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31605
Date

Vanessa Marakas

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT TRANSMITTAL

Sir:

1. Transmitted herewith is an amendment for this application.

STATUS

2. Applicant is

☐ a small entity.

☒ other than small entity.

EXTENSION OF TERM

3. The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply.

(a) ☐ Applicant petitions for an extension of time under 37 CFR 1.136

Applicant(s): Kyoung-hwan Kwon, *et al.*
Serial Number: 10/671,105

	Extension (months)	Fee for other than small entity	Fee for small entity
☐	one month	$120.00	$60.00
☐	two months	$450.00	$225.00
☐	three months	$1,020.00	$510.00
☐	four months	$1,590.00	$795.00

Fee $ _____

If an additional extension of time is required, please consider this a petition therefor.

☐ An extension for _____ months has already been secured and the fee paid therefor of $ _____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request $ _____

OR

(b) ☒ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition for extension of time.

FEE FOR CLAIMS

4. The fee for claims (37 CFR 1.16(b)-(d)) has been calculated as shown below:

CLAIMS AS AMENDED						
	(1)		(2)	(3)		
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT NUMBER EXTRA	RATE	FEE
TOTAL CLAIMS	16	minus	27	0	x $50	$0
INDEPENDENT CLAIMS	5	minus	6	0	x $200	$0
MULTIPLE DEPENDENT CLAIM ADDED	No				$360	
				TOTAL		$0
If applicant has small entity status under 37 CFR 1.9 and 1.27, then divide total fee by 2 and enter amount here.				SMALL ENTITY TOTAL		

Applicant(s): Kyoung-hwan Kwon, *et al.*
Serial Number: 10/671,105

(c) ☒ No additional fee for claims is required.

OR

(d) ☐ Total additional fee for claims required $_____

FEE PAYMENT

5. ☐ Attached is a check in the sum of $_____
☐ Charge Deposit Account No. _____ ___ the sum of $ _____.
A duplicate of this transmittal is attached.

Respectfully submitted,

Date: March 16, 2005

Mills & Onello LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900
Facsimile: (617) 742-7774
J:\SAM\0474\restriction-2\amendmenttransmittal.wpd

Anthony P. Onello, Jr.
Registration Number 38,572
Attorney for Applicant

PATENT
Attorney Docket No.: SAM-0474

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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3/16-05
Date

Vanessa Marakas

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Alexandria, Virginia 22313-1450

RESPONSE TO RESTRICTION REQUIREMENT WITH PRELIMINARY AMENDMENT

Sir:

In response to the Restriction Requirement dated February 17, 2005 in the above-referenced patent application, the Applicants hereby elect Group III, including claims 16-21, without traverse.

Prior to prosecution on the merits, please amend the application as follows:

Amendments to the Specification begin on page 2 of this paper

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 10 of this paper.

Amendments to the Specification:

Please replace the Title with the following amended Title:

SEMICONDUCTOR DEVICE COMPRISING FREQUENCY MULTIPLIER OF EXTERNAL CLOCK AND OUTPUT BUFFER OF TEST DATA AND SEMICONDUCTOR TEST METHOD

Amendments to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. - 27. (Canceled)

28. (New) A semiconductor device comprising:

a frequency multiplier at an input terminal of the semiconductor device that receives a clock signal having a predetermined frequency, and that generates a first internal clock signal having a frequency that is greater than the predetermined frequency,

a latency controller that controls a latency of the semiconductor device in response to the first internal clock signal and that generates a second internal clock signal according to the latency control result,

a data output buffer that outputs test output data for the semiconductor device in response to the first and second internal clock signals,

wherein the frequency multiplier comprises:

a first pulse signal generating circuit that receives a first clock signal and a second clock signal having the same frequency and that generates a first pulse signal having a first pulse width when a level of the first clock signal is greater than a level of the second clock signal,

a second pulse signal generating circuit that is enabled in response to a first control signal, and that generates a second pulse signal having a second pulse width when a level of a received reference voltage is greater than a level of the first clock signal, and

an OR circuit that receives the first pulse signal and the second pulse signal, that logically sums the first pulse signal and the second pulse signal, and that outputs the logically summed signal as the first internal clock signal.

29. (New) The semiconductor device of claim 28, wherein the first pulse signal

generating circuit comprises:

a first differential amplifier that receives the first clock signal and the second clock signal, and that senses and amplifies a difference between the first clock signal and the second clock signal; and

a first logic circuit that receives an output signal of the first differential amplifier and that generates the first pulse signal in response to the output signal of the first differential amplifier.

30. (New) The semiconductor device of claim 28, wherein the second pulse signal generating circuit further comprises:

a second differential amplifier that is enabled in response to the first control signal, and that senses and amplifies a difference between the reference voltage and the first clock signal; and

a second logic circuit that receives an output signal of the second differential amplifier and that generates the second pulse signal in response to the output signal of the second differential amplifier.

31. (New) The semiconductor device of claim 28, wherein the data output buffer comprises:

N flip flops, connected in series with each other, that each receive the first internal clock signal, including: a first flip flop that receives data to be output from the semiconductor device and that outputs data in synchronization with the first internal clock signal; and second through Nth flip flops that each receive an output signal of a preceding flip flop in the series and that output the data of the preceding flip flop in synchronization with the first internal clock signal;

an OR circuit that receives output signals of the N flip flops, logically sums the output signals, and outputs the summation signal; and

an output circuit that is synchronized with the second internal clock signal and outputs the summation signal of the OR circuit,

wherein the clock signal frequency of the first internal clock signal is N times greater than the clock signal frequency of the second internal clock signal.

32. (New) The semiconductor device of claim 28, wherein the first pulse signal and the second pulse signal have the same pulse width.

33. (New) A semiconductor device comprising:

a frequency multiplier at an input terminal of the semiconductor device, that receives a clock signal having a predetermined frequency, and that generates a first internal clock signal having a frequency that is greater than the predetermined frequency,

a latency controller that controls a latency of the semiconductor device in response to the first internal clock signal and that generates a second internal clock signal according to the latency control result, and

a data output buffer that outputs test output data for the semiconductor device in response to the first and second internal clock signals,

wherein the frequency multiplier comprises:

a first pulse signal generating circuit that receives a first clock signal and a second clock signal having the same frequency and that generates a first pulse signal having a first pulse width when a level of the first clock signal is greater than a level of the second clock signal,

a second pulse signal generating circuit that is enabled in response to a first control signal and that generates a second pulse signal having a second pulse width when a level of a received reference voltage is greater than a level of the first clock signal,

a third pulse signal generating circuit that is enabled in response to a second control signal and that generates a third pulse signal having a third pulse width when a level of the second clock signal is greater than a level of the reference voltage,

a fourth pulse signal generating circuit that is enabled in response to the second control signal, and that generates a fourth pulse signal having a fourth pulse width when a level of the

reference voltage is greater than a level of the second clock signal, and

an OR circuit that receives the first pulse signal, the second pulse signal, the third pulse signal, and the fourth pulse signal and that outputs the first internal clock signal that is the logical sum of the first pulse signal, the second pulse signal, the third pulse signal, and the fourth pulse signal.

34. (New) The semiconductor device of claim 33, wherein the first pulse signal, the second pulse signal, the third pulse signal, and the fourth pulse signal have the same width.

35. (New) The semiconductor device of claim 33, wherein the first control signal is enabled in a dual edge mode and the second control signal is enabled in a quadrature edge mode.

36. (New) The semiconductor device of claim 33, wherein the data output buffer comprises:

N flip flops, connected in series with each other, that each receive the first internal clock signal, including: a first flip flop that receives data to be output from the semiconductor device and that outputs data in synchronization with the first internal clock signal; and second through Nth flip flops that each receive an output signal of a preceding flip flop in the series and that output the data of the preceding flip flop in synchronization with the first internal clock signal;

an OR circuit that receives output signals of the N flip flops, logically sums the output signals, and outputs the summation signal; and

an output circuit that is synchronized with the second internal clock signal and outputs the summation signal of the OR circuit,

wherein the clock signal frequency of the first internal clock signal is N times greater than the clock signal frequency of the second internal clock signal.

37. (New) The semiconductor device of claim 36, wherein the data output buffer

includes 4 flip flops that are connected in series with each other.

38. (New) The semiconductor device of claim 33, wherein the first clock signal has a frequency 4 times greater than the second clock signal.

39. (New) A method of testing a semiconductor device, the method comprising:

receiving a clock signal having a predetermined frequency and generating a first internal clock signal having greater frequency than the predetermined frequency,

controlling a latency of the semiconductor device in response to the first internal clock signal and generating a second internal clock signal according to the latency control result, and

outputting test output data for the semiconductor device using the first and second internal clock signals,

wherein generating the first internal clock signal includes:

receiving a first clock signal and a second clock signal and generating a first pulse signal having a first pulse width when a level of the first clock signal is greater than a level of the second clock signal,

generating, in response to a first control signal, a second pulse signal having a second pulse width when a level of a received reference voltage is greater than a level of the first clock signal, and

logically summing the first pulse signal and the second pulse signal and outputting the signal obtained by the summation as the first internal clock signal.

40. (New) A method of testing a semiconductor device, the method comprising:

receiving a clock signal having a predetermined frequency and generating a first internal clock signal having greater frequency than the predetermined frequency,

controlling a latency of the semiconductor device in response to the first internal clock signal and generating a second internal clock signal according to the latency control result, and

summation signal of the OR circuit,

wherein the clock signal frequency of the first clock signal is N times greater than the clock signal frequency of the second clock signal.

42. (New) The buffer of claim 41, wherein N equals 4 and the data output buffer includes 4 flip flops that are connected in series with each other.

43. (New) The buffer of claim 41, wherein the first clock signal has a frequency 4 times greater than the second clock signal.

Applicant(s): Kyoung-hwan Kwon, *et al.*
Serial Number: 10/671,105

REMARKS

In response to the Restriction Requirement dated February 17, 2005, the Applicants hereby elect Group III, including claims 16-21, without traverse. Please cancel claims 1-15 and 22-27 without prejudice to the filing of divisional applications..

Following the response to the Restriction Requirement, Group III claims 16-21 are pending in the application. Newly added claims 28-43 are commensurate with elected Group III. Entry of new claims 28-43 is respectfully requested. Former Group III claims 16-21 are canceled above.

The Title is amended above to reflect the elected Group III claims. Entry of the amended title is respectfully requested.

Closing Remarks

If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

Date: March 16, 2005

MILLS & ONELLO LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900
Facsimile: (617) 742-7774
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Anthony P. Onello, Jr.
Registration Number 38,572
Attorney for Applicant

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SUITE 605
BOSTON MA 02108

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